MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2016/2017

ECE4116 – DIGITAL COMPUTER DESIGN

(All Section / Groups)

31 MAY 2017
2:30 P.M – 4:30 P.M.
(2 Hours)

INSTRUCTION TO STUDENT

1. This examination paper consists of SIX (6) pages with FOUR (4) questions only.
2. Answer ALL questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) Boolean function F, expressed as the sum of its minterms, is

$$F(X,Y,Z) = \sum m(0,3,4,7)$$

F is to be implemented using a decoder.

i) Write the truth table.

[2 marks]

ii) Draw the circuit diagram.

[4 marks]

iii) Write the VHDL code for an entity that represents the function F.

[5 marks]

(b) Figure Q1b shows the Finite State Machine (FSM) chart of a sequential circuit with 2 inputs, W1 and W2, an output, Z.

(i) Draw the Algorithmic State Machine (ASM) chart for the circuit based on the FSM.

[6 marks]

(ii) Design the circuit using the One Flip-Flop Per State technique. Draw the circuit diagram.

[8 marks]

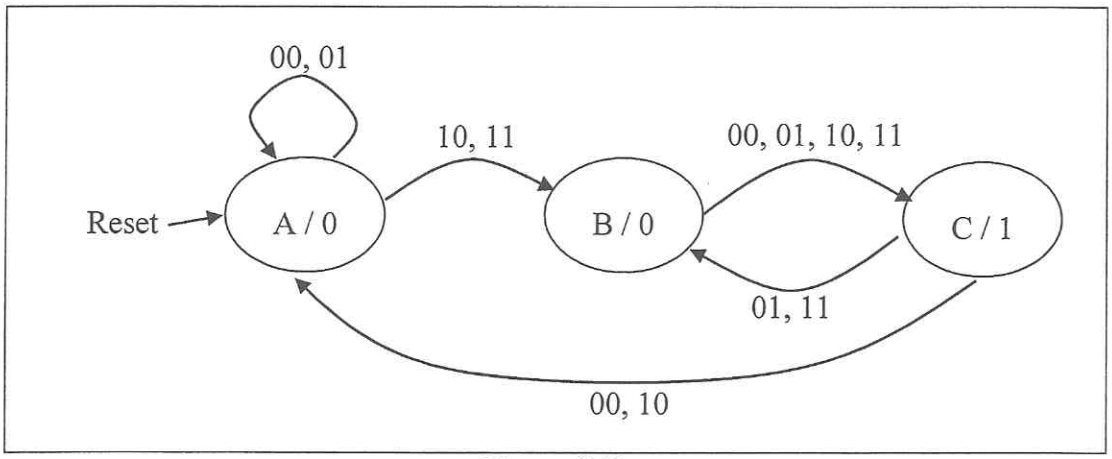

Figure Q1b

Continued...

Question 2

(a) A digital system has TWO (2) registers, RA and RB, and control signals $C1$, $C2$, and $C3$. The control signals control the following register transfers:

$$C1: RA \leftarrow RB$$
$$C2: RA \leftarrow \overline{RB}$$
$$C3: RA \leftarrow RA + RB \quad ; \text{(logical } OR\text{)}$$

All the control signals are mutually-exclusive. When none are '1', no transfers occur. Design the logic circuit to implement the register transfers and draw the one-bit slice logic diagram.

[10 marks]

(b) (i) List any TWO (2) types of microoperations.

[2 marks]

(ii) Give one example of a microoperation for each of the types listed in part (i).

[2 marks]

(c) Consider a 128K×32 RAM chip.

(i) Compute the number of address lines of the RAM chip.

[1 marks]

(ii) Compute the size of the decoder required if the RAM chip uses **a single decoder** to decode the address lines.

[2 marks]

(iii) Compute the number of inputs of the row and column decoders if the RAM chip uses **coincident selection scheme** decoding.

[6 marks]

(iv) Compare, in terms of total decoder outputs, between using a single decoder and using coincident selection decoding, for address decoding.

[2 marks]

Continued...

Question 3

(a) Figure Q3a shows the function table of an arithmetic circuit. The inputs are 16-bit data A and B, and control signals $S0$ and $S1$. The output is a 16-bit value, F.

$S1$	$S0$	Function
0	0	$F = A$ (transfer)
0	1	$F = A + B$ (addition)
1	0	$F = A + \bar{B} + 1$ (subtraction)
1	1	$F = A + 1$ (increment)

Figure Q3a

The arithmetic circuit consists of a parallel adder with 2 data inputs, X and Y, an output, S, carry-in, Cin, and carry-out, $Cout$. Data A connects to X input and data B connects to Y input. Y input requires additional logic to implement the functions given in Figure Q3a.

i) Write the truth table for X, Y, and Cin input values in terms of A, B, $S0$, and $S1$.

[4 marks]

ii) Based on the truth table in (i) write the Boolean expressions for X, Y and Cin inputs.

[4 marks]

iii) Y input logic is to be implemented using a 4-to-1 multiplexer. Draw the complete circuit block diagram for the arithmetic circuit.

[6 marks]

(b) A hypothetical computer has ONE (1) general-purpose register, $R1$. The instruction set includes instructions MOV (move), ADD (add), SUB (subtract), MUL (multiply) and DIV (divide). All instructions specify TWO (2) memory addresses, where the first one is an operand (if applicable) and the destination. Given the arithmetic expression:

$$A = (P - Q) + R/S$$

where A, P, Q, R, S denote memory addresses,

i) Write the instructions to evaluate the arithmetic expressions and store the result in memory location A.

[5 marks]

ii) State the number of memory accesses required. Subsequently, state how the number of memory accesses can be reduced.

[2 marks]

Continued...

(c) A simple computer uses 16-bit wide data and hardwired control. Figure Q3c shows the format of its immediate-mode instruction.

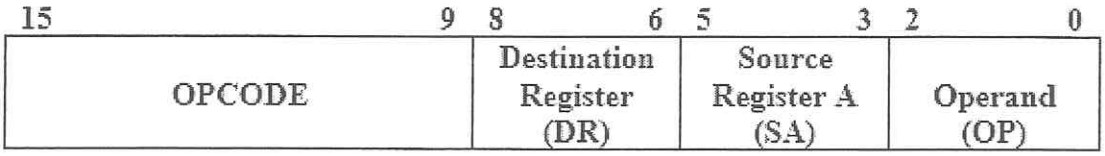

Figure Q3c

The 3-bit operand (OP) in the instruction must be extended to 16 bits in the control unit. State the TWO (2) operations that can be used to achieve this and briefly describe the difference between them.

[4 marks]

Question 4

(a) A pipelined datapath breaks the conventional datapath into several parts using pipeline platforms in-between the parts.

i) Describe how a pipelined datapath results in faster execution compared to conventional datapath.

[2 marks]

ii) A 4-stage pipeline will never achieve an improvement factor of 4. Describe the reason(s).

[4 marks]

(b) A hypothetical RISC machine employs a typical 4-stage pipeline. The following sequence of instructions is executed.

```
MOVA    R1, R5
SLT     R2, R4, R1
BNZ     R2, 25
MOVA    R5, R8
```

(i) Draw the pipeline execution diagram to show the execution of the instructions. Subsequently, identify all hazards and specify what type they are.

[7 marks]

(ii) Describe the methods to resolve the hazards identified in part (i).

Continued...

[6 marks]

(c) CISC machines have complex instructions, some of which require more than one execution cycle to complete. This characteristic makes it unsuitable for the standard pipelining.

i) Describe the modification that allows the implementation of a 4-stage pipeline for a CISC machine.

[2 marks]

ii) Draw the block diagram to show the implementation.

[4 marks]

End of Paper